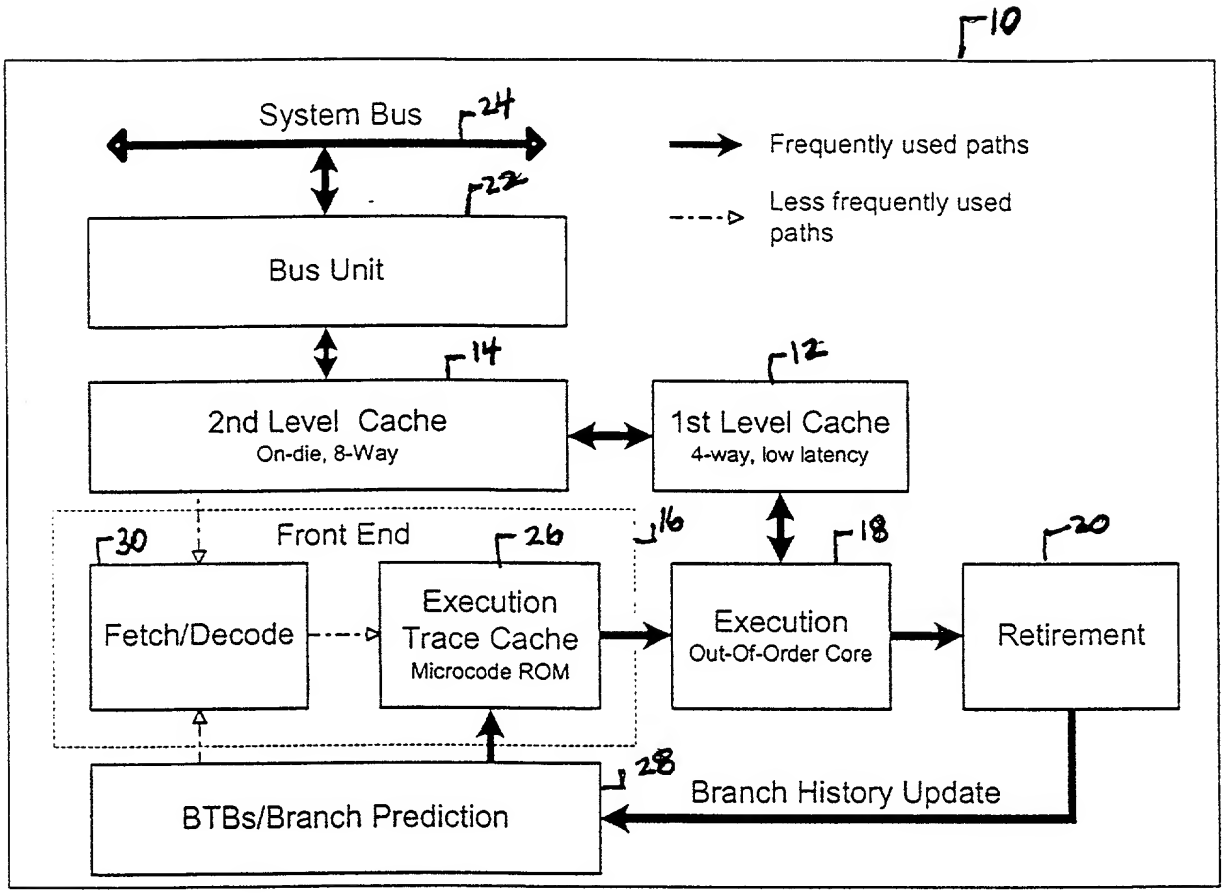
10
System Bus
24
Frequently used paths
Less frequently used paths
22
Bus Unit
14
12
2nd Level Cache
On-die, 8-Way
1st Level Cache
4-way, low latency
16
Front End
30
26
18
20
Fetch/Decode
Execution
Trace Cache
Microcode ROM
Execution
Out-Of-Order Core
Retirement
28
Branch History Update
BTBs/Branch Prediction

FIG. 1

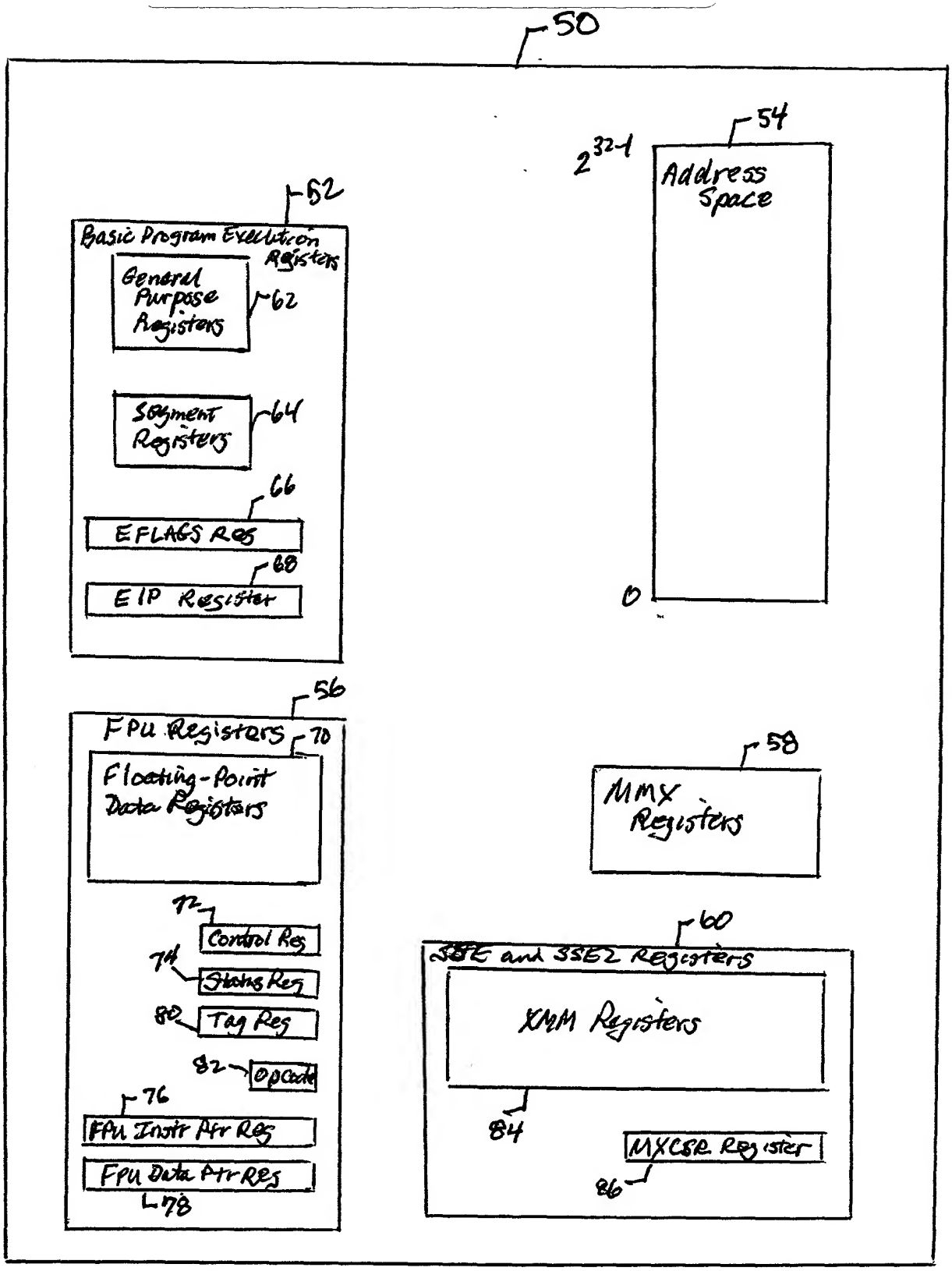
50
54
$2^{32}-1$
Address Space
0
52
Basic Program Execution Registers
General Purpose Registers
62
Segment Registers
64
66
EFLAGS Reg
68
EIP Register
56
FPU Registers
70
Floating-Point Data Registers
72
Control Reg
74
Status Reg
80
Tag Reg
82
Opcode
76
FPU Instr Ptr Reg
FPU Data Ptr Reg
78
58
MMX Registers
60
SSE and SSE2 Registers
XMM Registers
84
MXCSR Register
86

FIG. 2

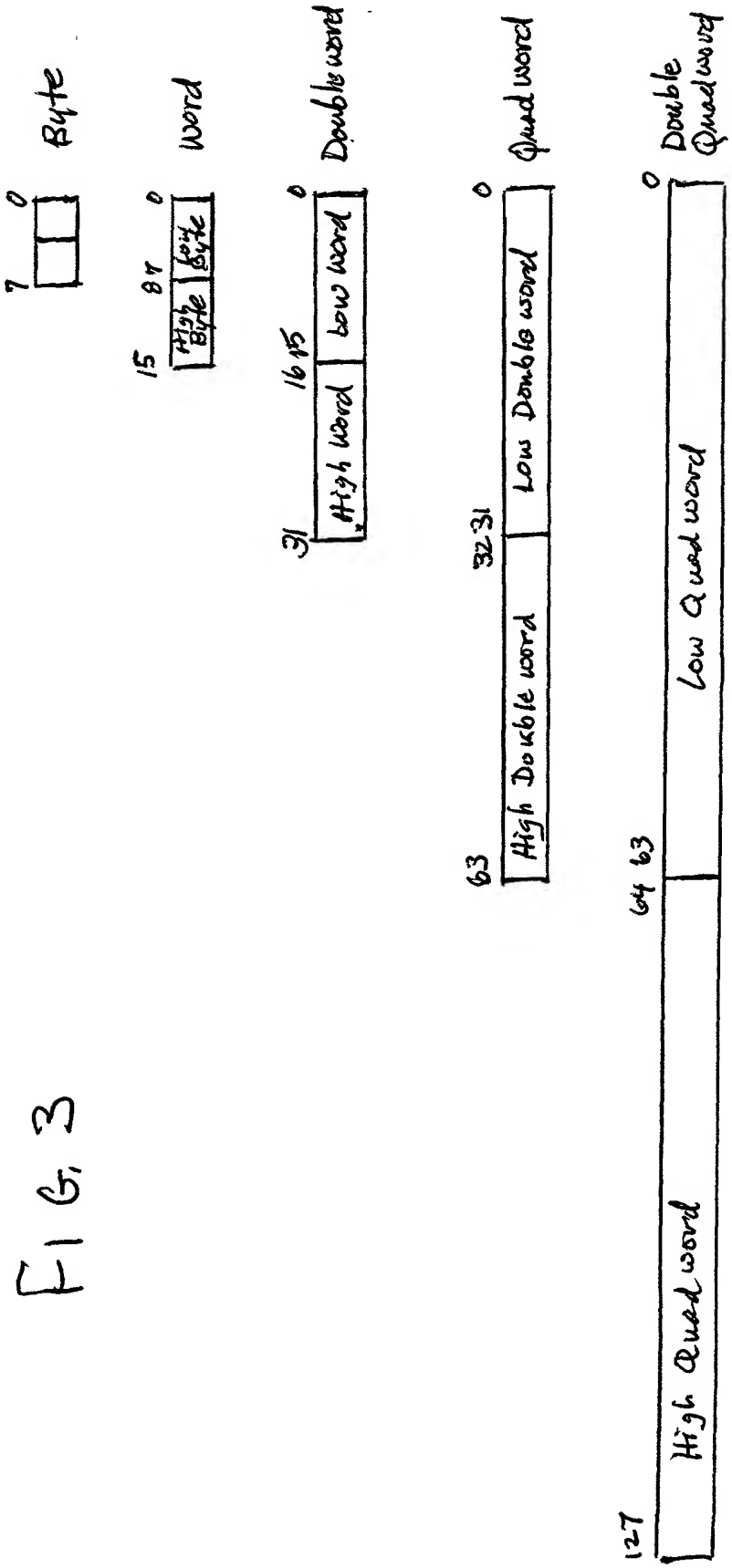
7
0
Byte
15
8 7
0
High Byte
Low Byte
Word
31
16 15
0
High word
Low word
Double word
63
32 31
0
High Double word
Low Double word
Quad word
127
64 63
0
High Quad word
Low Quad word
Double Quad word

FIG. 3

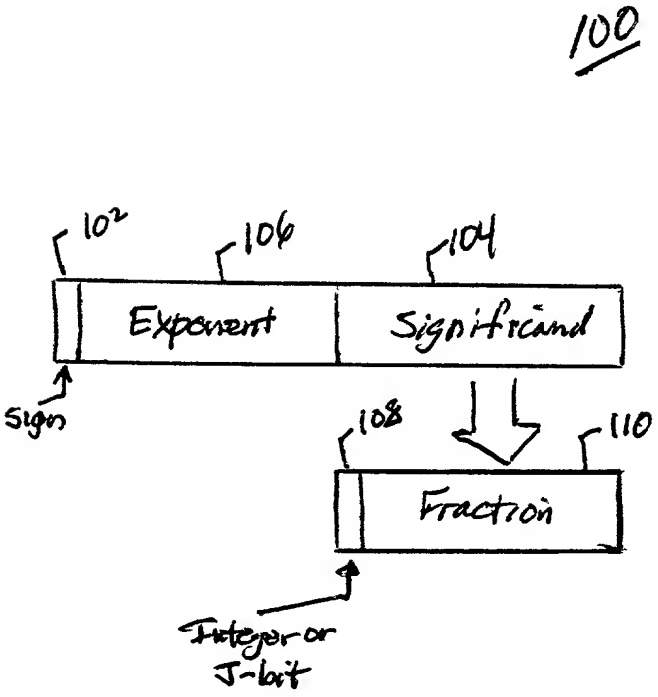
100
102
106
104
Exponent
Significand
Sign
108
110
Fraction
Integer or J-bit

FIG. 4

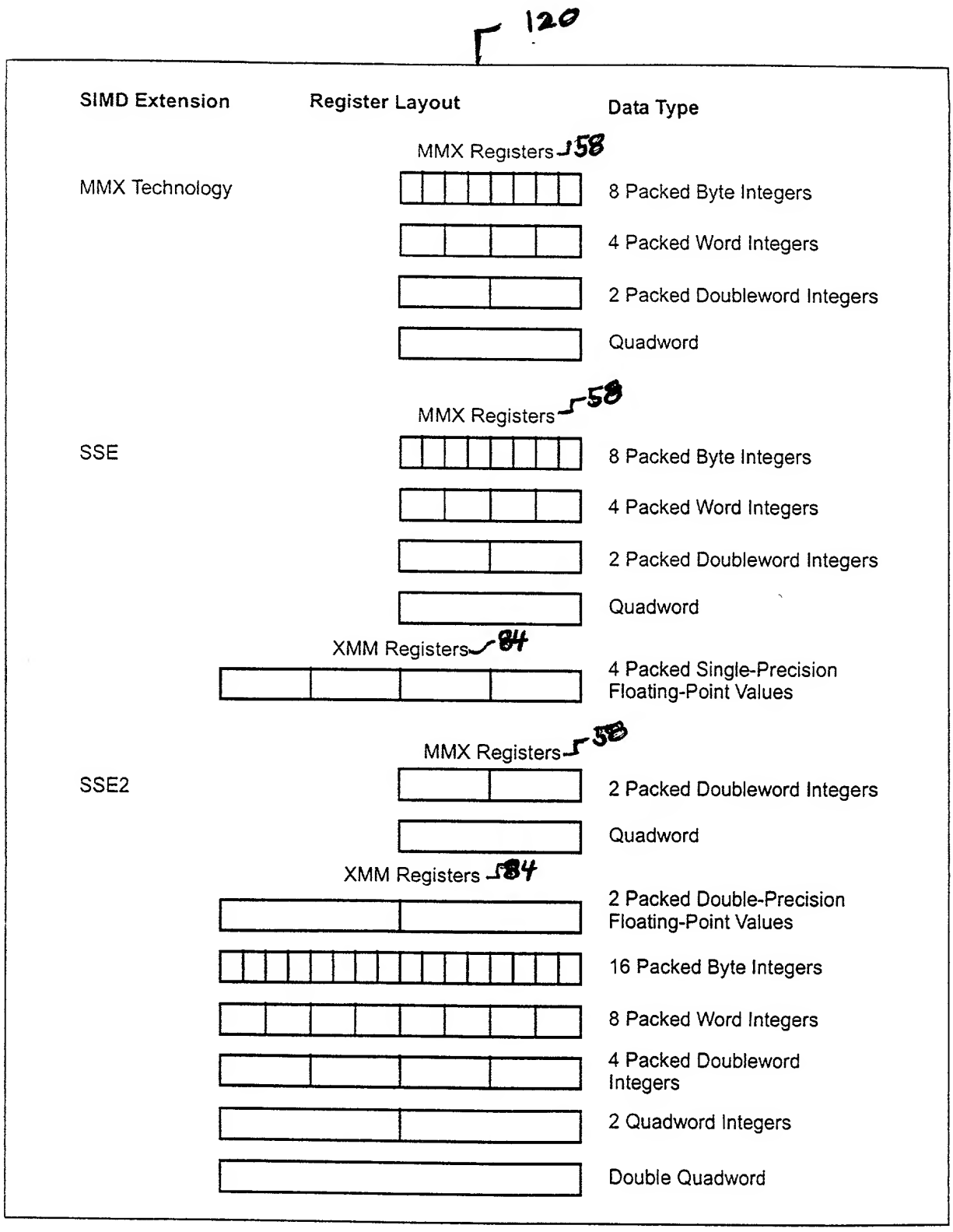
120
SIMD Extension
Register Layout
Data Type
MMX Registers 158
MMX Technology
8 Packed Byte Integers
4 Packed Word Integers
2 Packed Doubleword Integers
Quadword
MMX Registers 58
SSE
8 Packed Byte Integers
4 Packed Word Integers
2 Packed Doubleword Integers
Quadword
XMM Registers 84
4 Packed Single-Precision Floating-Point Values
MMX Registers 58
SSE2
2 Packed Doubleword Integers
Quadword
XMM Registers 84
2 Packed Double-Precision Floating-Point Values
16 Packed Byte Integers
8 Packed Word Integers
4 Packed Doubleword Integers
2 Quadword Integers
Double Quadword

FIG. 5